Electronics II

Lecture 08
FET Small Signal Analysis

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Previous Lecture

- BJT Small Signal Analysis
  - Small Signal Analysis of CE Emitter Bias Configuration.
  - Small Signal Analysis of Emitter Follower Configuration.
  - Small Signal Analysis of Common Base Configuration.

Session Overview

Topic	FET Small Signal Analysis
Concepts	Trans- conductance, Input Impedance, Output Impedance, FET AC Equivalent Circuit, JFET Fixed Bias Configuration Small Signal Analysis.
Recommended Reading	Sections 9.1, 9.2 & 9.3of [1]
Keywords	Emitter Follower, Common Base, Small Signal, BJT, Fixed Bias.

FET Amplifiers

- Good Voltage Gain.
- High Input Impedance.
- Less power consumption.
- Work with wide range of frequencies.
- Small size and weight.
- Trans- conductance factor (g_m) is the counterpart of amplification factor (β).
- Current gain: Undefined (Why)
- Common Source
  - Most popular.
  - Characterized by inverted amplified signal.
- Common Drain.
  - Characterized by unity gain and no inversion.
- Common Gate.
  - Characterized by gain with no inversion.
- Input Impedance is very high.
- Output Impedance is comparable to that of BJT.

FET Small Signal Model

- FET is a voltage controlled device, so the relationship between the V_{GS} and I_D is defined as

  $\Delta I_D = g_m \Delta V_{GS}$

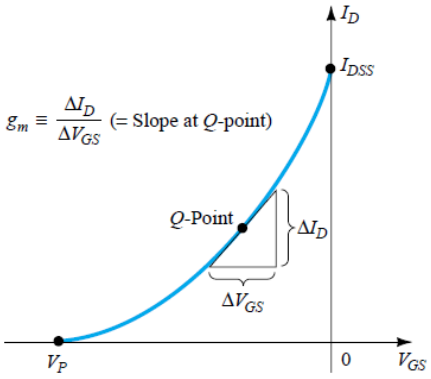
  where

  I_D= controlled current.

  V_{GS}= Controlling Voltage.

- g_m is called trans- conductance, where the term trans is used to describe the relationship between input and output.

- $g_m = \Delta I_D / \Delta V_{GS}$
- $g_m = m = \Delta y / \Delta x = \Delta I_D / \Delta V_{GS}$



Robert L. Boylestad, *Electronic Devices and Circuit Theory*, 8th Edition, Pearson Education Inc, ISBN: 81-7808-590-9.

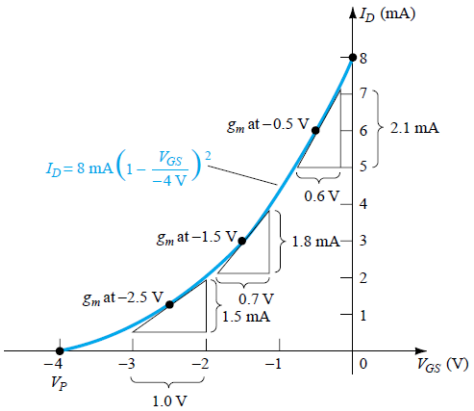
FET Small Signal Model

- *Example 9.1 (Boylestad):* Determine the magnitude of g_m for a JFET with I_{DSS}= 8mA and V_P= -4V at following DC bias points

  (a) V_{GS}= -0.5V.

  (b) V_{GS}= -1.5V.

  (c) V_{GS}= -2.5V.



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FET Small Signal Model

- ***Mathematical Definition of gm:***

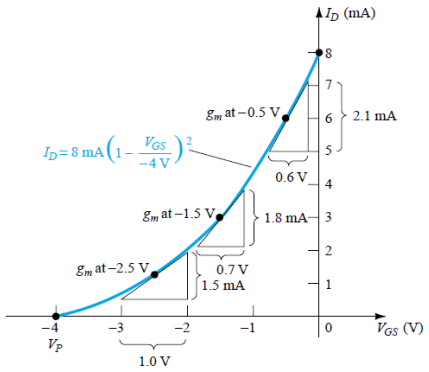
- The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

- $g_m=(2I_{DSS}/|V_P|)[1-V_{GS}/V_P]$

- $g_{m0}=(2I_{DSS}/|V_P|)$
- $g_m= g_{m0}[1-V_{GS}/V_P]$

FET Small Signal Model

- Example 9.2 (Boylestad): For the JFET of Example 9.1,
  - Find the max. value of g_m.
  - Find the value of g_m at each operating point of Example 9.1 using mathematical formula and compare with the graphical results.



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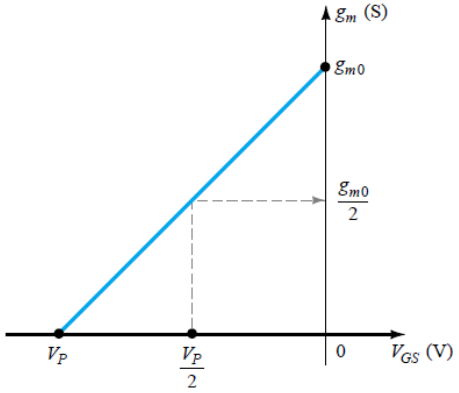
FET Small Signal Model

- g_m vs V_{GS}



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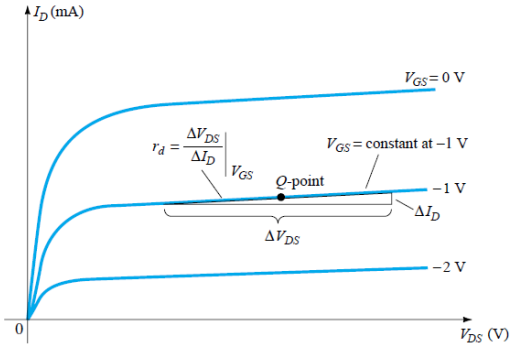
FET Small Signal Model

- Input Impedance
  $Z_{i\,(FET)} = \infty\Omega$.
  Typical Values
  JFET= 1000MΩ
  MOSFET= 10^{12} to 10^{15} Ω
- Output Impedance
  Zo (FET)= $r_d = 1/y_{os}$.
  $r_d = (\Delta V_{DS}/\Delta I_D)|_{V_{GS}=\text{constant}}$.



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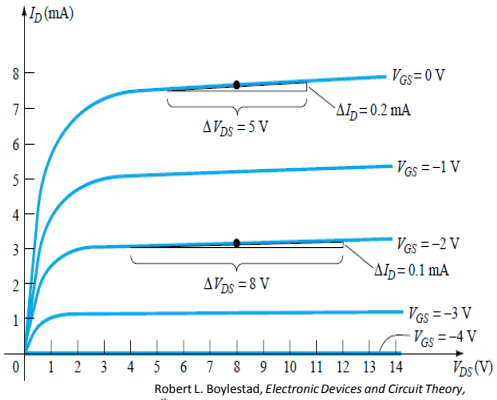
FET Small Signal Model

- *Example 9.5(Boylestad):* Determine the output Impedance for the given FET curves for
  - V_{GS}= 0V (at V_{DS}= 8V).
  - V_{GS}= -2V (at V_{DS}= 8V).



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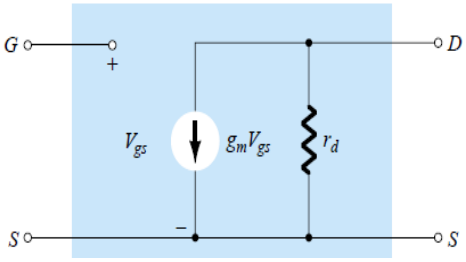
FET Small Signal Model

- FET AC Equivalent Circuit
- I_d represented as a voltage controlled current source $g_m V_{gs}$ with 180 degrees phase shift.
- Input impedance is represented as an open circuit at input terminals.
- Output impedance is represented by rd from drain to source.



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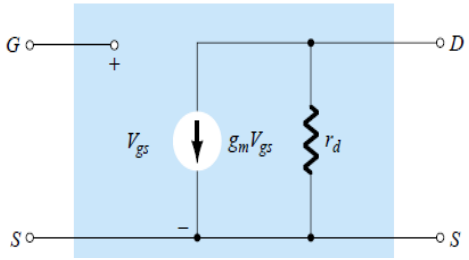
FET Small Signal Model

- *Example 9.6 (Boylestad):* Sketch FET ac Equivalent Model for y_{fs}= 3.8mS and y_{os}= 20µS.



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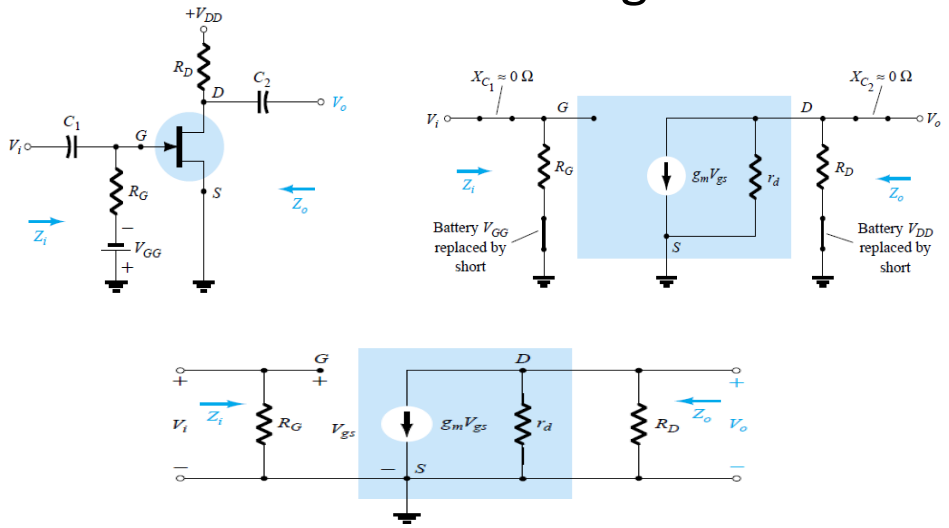
JFET Fixed Bias Configuration



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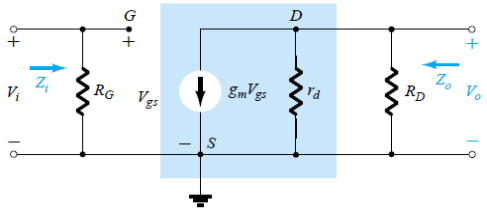
JFET Fixed Bias Configuration



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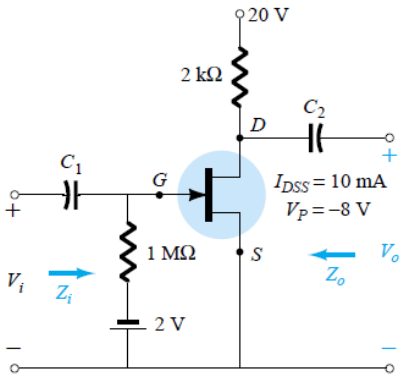
JFET Fixed Bias Configuration

- *Example 9.7 (Boylestad):* The given fixed bias configuration has an operating point defined by V_{GSQ}= -2V, I_{DQ}=5.625mA and I_{DSS}= 10mA and V_P= -8V.

  Assume y_{os}= 40µS, determine
  - gm
  - Zi
  - Zo
  - Av
  - Av (Ignoring the effects of rd)



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References

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